InTe-based Multi-Stack Selector-Only Memory

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We introduce an advanced multi-stack In-Te selector-only memory (SOM) device exhibiting ultra-low power consumption, exceptional reliability, and superior operational endurance [1-3]. Conventional selector-only memories typically employ selenium (Se)-based materials, which suffer from performance instability and high operational currents due to their complex multi-element compositions [4]. To address these limitations, we developed a simplified binary In-Te system that significantly enhances both power efficiency and reliability through optimized elemental bonding and controlled trap engineering.

Our innovative multi-stack structure consists of strategically arranged In-rich, optimized, and Te-rich layers, carefully designed to significantly reduce the required write current (I_{write}) down to an ultra-low level of 10 μA. This architectural strategy ensures notably improved energy efficiency while simultaneously providing a substantial memory window (~1 V) with minimal operational variability. Comprehensive characterization via X-ray photoelectron spectroscopy (XPS), Raman spectroscopy, and density functional theory (DFT) simulations validated the underlying mechanisms driving the exceptional performance. These analyses revealed that the optimized In-Te heteropolar bonds and the precise distribution of charged hole traps (Te^{2-}) critically enhance the device's overall reliability and functionality.

Experimental data confirm that our multi-stack In-Te SOM achieves outstanding endurance, consistently performing reliable read and write operations for up to 10^{10} cycles at the significantly reduced current level of 10 μA. The device's remarkable structural robustness and performance reliability are primarily attributed to the strong ionic-like In-Te bonds, which effectively resist bond breaking and maintain stable trap dynamics, enabling sustained SOM behavior. Comparative tests with conventional single-stack structures further illustrate the clear superiority of the multi-stack architecture, highlighting stable, error-free switching even under dramatically reduced operational currents.

In summary, this study demonstrates a novel multi-stack In-Te based selector-only memory design that achieves improvements in power efficiency (10 μA operational current), high reliability, and extraordinary endurance capabilities (10^{10} cycles). These advancements represent a significant leap forward in selector-only memory technology, providing a highly viable and promising solution for future applications in high-density memory configurations, such as 3D vertical cross-point arrays (V-XPA). Our findings underscore the potential for widespread adoption of this advanced SOM architecture in next-generation semiconductor memory technologies.

References

[1] S. Ban, J. Lee, T. Kim, and H. Hwang, in *Proc. IEEE Symp. VLSI Technol. Circuits*., Jun. 2023

[2] Y. Seo, D. Kim, L. Jung, J. Lee, O. Kwon, C. Baek, Y. Park, T. Lee and H. Hwang., in *Proc. IEEE Symp. VLSI Technol. Circuits* Jun. 2025

[3] S Ban, J Lee, Y Seo, W Lee, T Kim, H Hwang, *Adv. Electronic Materials*, vol. 11, 2400665, 2025

[4] J. Lee, T. Ravsher, D. Garbin, S. Clima, R. Degraeve, A. Belmonte, H. Hwang, I. Lee, *IEEE Journal of the Electron Devices Society, vol. 13, pp. 362-365, 2025*

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